Digital Scalar Pulsewidth Modulation for Open-End Winding Induction Motor Drives

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***Abstract*—In power electronics, research on modulation techniques and converter topologies has been carried out aiming at greater efficiency in energy conversion process for industry applications in electric machine drives. As an alternative to the classic drive systems based on a two-level (2L) inverter, feeding induction motors via open-end windings (OEWs) has become an interesting drive solution for improving output waveform quality and reducing switching losses. This paper aims to study and implement improvement on conversion process of the OEW-motor drive, by a dual 2L inverter, from a digital scalar pulsewidth modulation (PWM). Therefore, the dual-inverter system model was developed, so that was possible to identify the degrees of freedom that can be used to optimize the conventional carrier-based modulation technique, considering the waveform quality. After studying the systems, simulations were performed to compare the conventional and dual drive systems with the application of the conventional and proposed modulation techniques, respectively.**

Keywords— digital scalar pulsewidth modulation, dual inverter, open-end winding induction motor, variable-speed drives, power converter.

I. INTRODUCTION

Much of the electricity consumed in industries is associated with powering electric motors, especially variable speed electric machines, also known as variable-speed drives (VSDs). According to [1], efficiency has become a major figure of merit in recent industry context because of the economic benefits along with the importance of sustainability, which has led to a higher demand for VSDs. In general, researches in static power converters has been seeking more efficient conversion processes at a competitive cost. In view of this, researchers have joined efforts in the technological development of converter topologies and modulation techniques that can minimize conversion losses.

Therefore, when it comes to three-phase electric drives, supplying motor via open-end windings (OEWs) has become an interesting drive solution for produce multilevel voltages from topologies with fewer levels, such as from a dual two-level (2L) inverter, as shown in Fig. 1, [2]–[6]. In the OEW configuration, stator windings allow converters (conventional or multilevel topologies) to be connected on both side of the machine terminals. This type of configuration is quite usual for driving three-phase induction motors, in which the stator windings are designed to allow delta or wye connection.

In an OEW drive system, each inverter may be powered by a dc source whose rated voltage is half that required by a conventional drive system, e.g., a wye-connected motor driven by a 2L inverter, as shown in Fig. 2. The series association of inverters gives the system a fault tolerance capability due to inverter redundancy, not to mention that the output form quality is superior to the conventional system. Moreover, besides reducing the voltage stress at switching devices and increasing even more the output voltage quality, having a dual 2L topology increases the number of space-vector combinations, making it possible to minimize shaft voltage [2] and to balance dc capacitor voltages [3] by properly selecting the available redundancies. On the other hand, the drive system becomes more complex and its initial cost can be higher than the conventional system, due to the increased number of semiconductor devices.

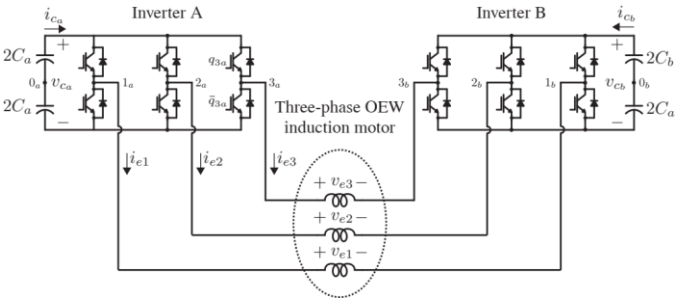

Fig. 1. Dual 2L inverter for driving a three-phase OEW motor induction.

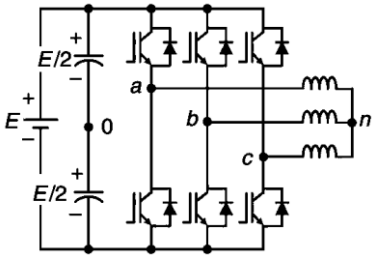

Fig. 2. Conventional three-phase inverter [7].

This paper aims to study and implement improvement on conversion process of the electric OEW motor drive from a digital scalar pulsewidth modulation (PWM). According to [8], in the scalar modulation techniques, the PWM pattern is determined from the instantaneous values of the converting voltages by simply manipulating the system equations, so that computation effort can be reduced. From an analysis of the

system model, the proposed PWM is implemented for generating the output voltage references to any power distribution of the dc links. The proposed modulation technique is a generalization of that described in [9], by using additional degrees of freedom of the system to improve the output waveform quality and reduce the switching losses, simultaneously.

II. System model

Analyzing the circuit meshes of Fig. 2, the phase voltages (v_{ej}) of the OEW machine can be determined by

$$v_{ej} = v_{ja} - v_{jb} \tag{1}$$

where $j = \{1, 2, 3\}$ denotes the system phase.

The voltages v_{ja} and v_{jb} represent, respectively, the output voltages of inverters A and B, thus succinctly presented by v_{jk} considering $k = a$ in reference to converter A and $k = b$ in reference to converter B. In addition, the three-phase pole voltages (v_{j0k}) of the inverters can be expressed in function of their respective voltages v_{jk} and the voltage at the '$0k$' pole of the respective DC buses, as follows:

$$v_{j0k} = v_{jk} - v_{0k} \tag{2}$$

For both inverters A and B, pole voltages v_{j0k} have two voltage levels and can be represented as a function of the switching states of the power switches (q_{jk}), where $q_{jk} = 1$ means switch on and $q_{jk} = 0$ means switch off. In addition, there is the complementary switching state represented by $\bar{q}_{jk} = 1 - q_{jk}$, which indicates the operation of the inverter lower switch. For example, the voltage v_{30a} assumes voltage value $+v_{ca}/2$ if $q_{3a} = 1$ and, $\bar{q}_{3a} = 0$ and assumes voltage value $-v_{ca}/2$ if $q_{3a} = 0$ and $\bar{q}_{3a} = 1$. Therefore, voltage v_{j0k} can be expressed by

$$v_{j0k} = (2q_{jk} - 1)\frac{v_{ck}}{2} \tag{3}$$

where v_{ck} represents the dc-link voltages, considering $\bar{q}_{jk} = 1 - q_{jk}$.

Therefore, by isolating v_{jk} in (2) and substituting (1), the voltages v_{ej} can be expressed by

$$v_{ej} = v_{j0a} - v_{j0b} - v_{0ba} \tag{4}$$

in which $v_{0ba} = v_{0b} - v_{0a}$ represents the differential mode voltage (DMV) (v_{DMV}) component of the system, as referred in [2].

Thus, for a balanced system, the sum of v_{ej} is null, as follows:

$$\sum_{j=1}^{3} v_{ej} = 0 \tag{5}$$

Thus, from (4) and (5), voltage v_{0ba} is defined by

$$v_{0ba} = \frac{1}{3}\sum_{j=1}^{3} v_{j0a} - \frac{1}{3}\sum_{j=1}^{3} v_{j0b} \tag{6}$$

$$\Rightarrow v_{\mathrm{DMV}} = v_{\mathrm{CMV}a} - v_{\mathrm{CMV}b} \tag{7}$$

in which $v_{\mathrm{CMV}a} = \frac{1}{3}\sum_{j=1}^{3} v_{j0a}$ and $v_{\mathrm{CMV}b} = \frac{1}{3}\sum_{j=1}^{3} v_{j0b}$.

As can be noticed in (6), the voltage v_{0ab} is the difference between the sum of the three-phase pole voltages of each converter. Each sum represents the common mode voltage (CMV) of each inverter, as in (7). Therefore, in an OEW drive system, the differential mode voltage is the difference between the individual common mode voltages, so that the resulting common mode voltage (v_{CMV}) is given by the sum, as follows:

$$v_{\mathrm{CMV}} = \frac{1}{2}(v_{\mathrm{CMV}a} + v_{\mathrm{CMV}b}) \tag{8}$$

Considering that dc links are separated and powered by isolated sources, the voltage distribution between dc links can be asymmetrical or symmetrical.

In an asymmetric scenario, the number of voltage levels can be maximized using switching states to generate intermediate levels. It is noteworthy that each dc link can be powered by isolated dc sources, but there is also the possibility of the system operating with a floating dc link. By operating with a floating dc link the number of isolated dc sources can be reduced, however, the maximum modulation index (m_a) value is restricted to maintain the floating capacitor voltage balance. In a symmetrical scenario, the number of redundant states available is greater than in an asymmetric scenario and can be used, for example, to i) equilibrate dc capacitor voltages in multilevel topologies; and ii) minimize leakage currents and other undesirable effects resulting from high frequency switching.

Thus, a power distribution factor (k_0) can be introduced to split the dc-link voltages symmetrically ($k_0 = 0.5$) or asymmetrically ($k_0 \neq 0{,}5$) such that $0 \leq k_0 \leq 1$. Thus, the voltages v_{ca} and v_{cb} can be expressed by

$$v_{ca} = k_0 V_{dc} \tag{9}$$

$$v_{cb} = (1 - k_0)V_{dc} \tag{10}$$

in which $V_{dc} = v_{ca} + v_{cb}$ is the total dc-link voltage required to power a machine with voltage amplitude equal to $V_e = \frac{1}{2} m_a V_{dc}$.

In addition, the voltage maximum generated by the converters can be calculated from (4), observing that

$$v_{ej} - v_{e\bar{j}} = (v_{j0a} - v_{\bar{j}0a}) - (v_{j0b} - v_{\bar{j}0b}) \tag{11}$$

with $j = \{1, 2, 3\}$ and $\bar{j} \neq j$. Since v_{ej} derives from a balanced three-phase system, i.e.,

$$v_{ej} = V_e \cos\left(\omega t - (j-1)\frac{2\pi}{3}\right) \tag{12}$$

the maximum amplitude of $v_{ej} - v_{e\bar{j}}$ is equal to $\sqrt{3}V_e$. Since $\max\{(v_{j0a} - v_{\bar{j}0a}) - (v_{j0b} - v_{\bar{j}0b})\} = V_{dc}$ and $\min\{(v_{j0a} - v_{\bar{j}0a}) - (v_{j0b} - v_{\bar{j}0b})\} = -V_{dc}$, for inverters to produce an

amplitude voltage V_e, is necessary to use a dc-link voltage V_{dc} with a minimum value of $\sqrt{3}V_e$.

III. Modulation technique

Since the pole voltage references (v_{j0k}^*) are known, those are applied to the PWM technique for generating the command pulse pattern for the power switches so that the conversion of direct voltage to alternating voltage is performed. The PWM technique has as objective to create a pulse sequence from the semiconductor operation imposing the phase voltage references (v_{ej}^*) on the machine, with constant average value during the switching period T_s. Therefore, references v_{ej}^* are defined by

$$v_{e1}^* = V_e^* \cos(\omega_e^* t) \tag{13}$$

$$v_{e2}^* = V_e^* \cos(\omega_e^* t - 2\pi/3\,) \tag{14}$$

$$v_{e3}^* = V_e^* \cos(\omega_e^* t - 4\pi/3\,) \tag{15}$$

where ω_e^* is the angular frequency reference of the machine and V_e^* is the voltage amplitude reference whose steady state value is $V_e^* = \frac{1}{2} m_a V_{dc}$ for a given value of m_a.

According to (2), the voltages v_{j0k}^* are expressed by

$$v_{j0k}^* = v_{jk}^* - v_{0k}^* \tag{16}$$

From (16), the references of the differential pole voltages (v_{rj}^*) can be introduced as follows:

$$v_{rj}^* = v_{j0a}^* - v_{j0b}^* \tag{17}$$

Thereby, it can be deduced from (4) that

$$v_{rj}^* = v_{ej}^* + v_{0ba}^* \tag{18}$$

As can be observed in (18), the component v_{0ba}^* is a degree of freedom of the system that can be used to generate an average voltage in the interval T_s equal to v_{ej}^*. Thus, voltage v_{0ba} can be controlled from a differential voltage apportionment factor (μ_0). For this, v_{0ba}^* is determined, extracting the instantaneous values of v_{ej}^* and considering the voltage limits $V_{dc}/2$ and $-V_{dc}/2$, by

$$v_{0ba\,\max} = \frac{1}{2} V_{dc} - \max\{v_{e1}^*, v_{e2}^*, v_{e3}^*\} \tag{19}$$

$$v_{0ba\,\min} = -\frac{1}{2} V_{dc} - \min\{v_{e1}^*, v_{e2}^*, v_{e3}^*\} \tag{20}$$

and, then, introducing the factor μ_0, established from $0 \le \mu_0 \le 1$, v_{0ba}^* is calculated by

$$v_{0ba}^* = \mu_0 v_{0ba\,\max} + (1 - \mu_0) v_{0ba\,\min} \tag{21}$$

This degree of freedom can result in pole voltages v_{j0k} with different waveforms continuous and discontinuous non-sinusoidal that do not affect the mean voltage of v_{ej}.

Furthermore, as in (16), the voltages v_{rj}^* are a linear combination of v_{j0k}^*, which depend on the respective values of v_{ck}, thus, it is possible to express v_{j0a}^* and v_{j0b}^* as a function of k_0, from (9) and (10), by

$$v_{j0a}^* = k_0 v_{rj}^* \tag{22}$$

$$v_{j0b}^* = -(1 - k_0) v_{rj}^* \tag{23}$$

As can be noticed in (22) and (23), another degree of freedom in each phase of the proposed system can be explored. Thereby, an auxiliary variable v_{jab}^* is added to improve the quality of the output waveform by generating intermediate voltage levels. To determine the voltage v_{jab}^*, it is necessary to set the maximum ($v_{jab\,\max}^*$) and minimum ($v_{jab\,\min}^*$) limits as a function of the voltage v_{rj}^* and as function of the voltage of each dc link, v_{ca} and v_{cb}, respecting the converter voltage capacity, according to (9) and (10). The $v_{jab\,\max}^*$ and $v_{jab\,\min}^*$ limits are composed of two components, one associated with converter A and one with converter B, as follows:

$$v_{j0a}^* = k_0 v_{rj}^* + v_{jab}^* \tag{24}$$

$$v_{j0b}^* = -(1 - k_0) v_{rj}^* + v_{jab}^* \tag{25}$$

in which

$$v_{jab\,\max}^* = \min\left\{k_0\left(\frac{1}{2}V_{dc} - v_{rj}^*\right), (1 - k_0)\left(\frac{1}{2}V_{dc} + v_{rj}^*\right)\right\} \tag{26}$$

$$v_{jab\,\min}^* = \max\left\{k_0\left(-\frac{1}{2}V_{dc} - v_{rj}^*\right), (1 - k_0)\left(-\frac{1}{2}V_{dc} + v_{rj}^*\right)\right\} \tag{27}$$

Once established the limits of v_{jab}^*, as in (26) and (27), a differential pole voltage apportionment factor (μ_j) can introduced, which is comprised within $0 \le \mu_j \le 1$. Therefore, the voltage v_{jab}^* is given by

$$v_{jab}^* = \mu_j v_{jab\,\max} + (1 - \mu_j) v_{jab\,\min} \tag{28}$$

Note that the inclusion of this new component v_{jab}^* can modify the pole voltages, resulting in several output waveforms, depending on the value assigned to the factor μ_j that can be used to maximize the number of voltage levels and thus improve the output waveform quality.

The proposed PWM technique was evaluated from a comparison of the dual-inverter system (cf. Fig. 1) with the conventional system (cf. Fig. 2), in terms of semiconductor losses and output waveform quality by means of harmonic distortion. In this paper, the PWM technique used for conventional topology is based on that proposed in [7] was used, considering $\mu_0 = 0.5$. For dual-inverter topology, the converters can be controlled independently, being possible to use the conventional PWM technique in each converter. However, it is noteworthy that the carriers used in the modulation must be 180° for the generation of correct pulse pattern in a way that the switching of the converters to be complementary.

IV. Simulation results

To validate the PWM technique described in the previous section, the conventional and dual-inverter systems were

simulated in the PSIM software, considering the steady-state operation. In the simulation, both converters fed a 12-Ω and 4-mH three-phase RL load (emulating the steady-state characteristics of an induction motor) with a rated voltage of 380 V and a frequency of 60 Hz, operating at a switching frequency of 3 kHz, symmetrical apportionment factor (i.e., $\mu_0 = 0.5$), total dc-link voltage of 540 V (i.e., $m_a = 1.15$). In the case of the dual-inverter topology, separate and symmetrical dc links were considered (i.e., $k_0 = 0.5$). In Fig. 3 and Fig. 4, the simulation results of the conventional systems are presented, while in Fig. 5 and Fig. 6, the simulation results of the dual-inverter systems are presented.

In the upper traces of Fig. 3, the curves of the reference voltage v_{10}^* (red trace) of the conventional system and the PWM carrier can be observed (blue trace). Those curves are compared to generate the PWM pattern, resulting in the pole voltage curve v_{10} (red trace) illustrated in the lower traces of Fig. 3.

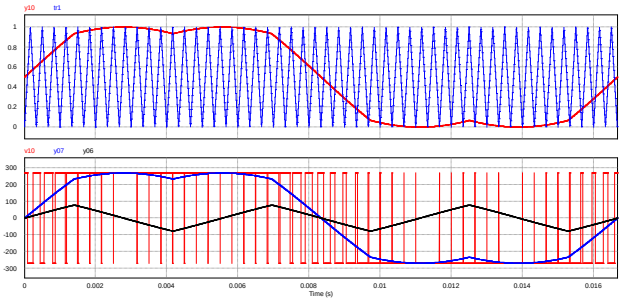

Fig. 3. Simulation results of the conventional system regarding the implementation of the conventional PWM technique. Upper traces: normalized reference of pole voltage (red) and triangular carrier (blue). Bottom traces: pole voltage (red), pole voltage reference (blue) and zero sequence voltage (black).

In the upper traces of Fig. 4, the reference v_{e1}^* (blue trace) and the phase voltage v_{e1} (red trace) applied to the machine with 5 voltage levels can be observed. From the traces illustrated below, the three-phase currents i_{ej} can be observed, presenting a sine waveform with low harmonic content.

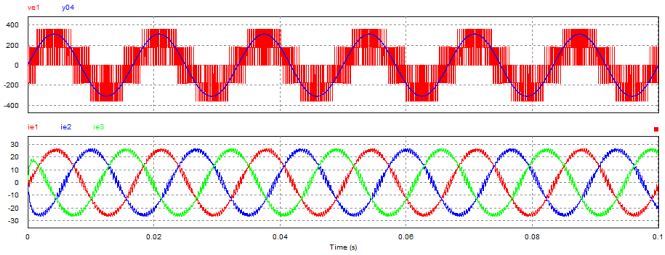

Fig. 4. Simulation results of the conventional system regarding the output signals. Upper traces: phase voltage (red) and the voltage reference (blue). Bottom traces: three-phase currents.

In the upper traces of Fig. 5, the carriers of the A and B converters (red and blue traces, respectively) of the dual-inverter system are illustrated. In addition, the references for pole voltages v_{10a}^* and v_{10b}^* (green and magenta traces, respectively) can also be observed.

Each carrier is compared to its respective reference voltage generating the proposed PWM pulse pattern, resulting in pole voltages v_{10a} and v_{10b}. In the lower traces of Fig. 5, the pole voltage v_{10a} (red trace) and its reference v_{10a}^* (blue trace) of converter A can be observed. It is worth mentioning that only the pulse pattern of converter A is shown, because the converter B has a similar pattern.

Note that the pole voltage reference clamps the pole voltage, causing the power switches to switch for a time and then switch off. In addition, the reverse-blocking voltages are smaller due the voltage in the dc link of each converter is half of the required voltage in the conventional system. From the proposed PWM technique, the power switches only commutate to each fundamental semicycle, reducing the total losses in the switches.

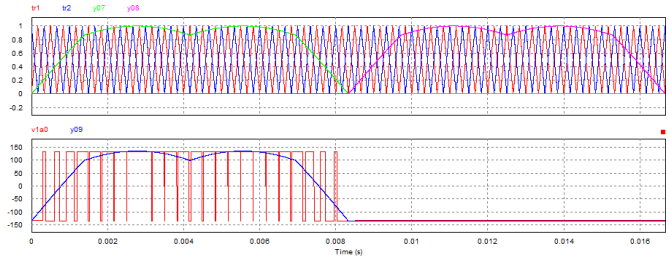

Fig. 5. Simulation results of the dual-inverter system regarding the implementation of the PWM technique. Upper traces: pole voltage reference of converter A (green), triangular carrier with 0º (red), pole voltage reference of converter B (magenta) and triangular carrier with 180º (blue). Bottom traces: pole voltage of converter A (red) and its voltage reference (blue).

In the upper traces of Fig. 6, the reference v_{e1}^* (blue trace) and the phase voltage v_{e1} (red trace) applied to the machine by the proposed topology with 9 voltage levels can be observed. Thus, the waveform presents a better quality than conventional systems. As a result, the traces illustrated below of the three-phase currents i_{ej} are observed, presenting a lower presence of harmonic content.

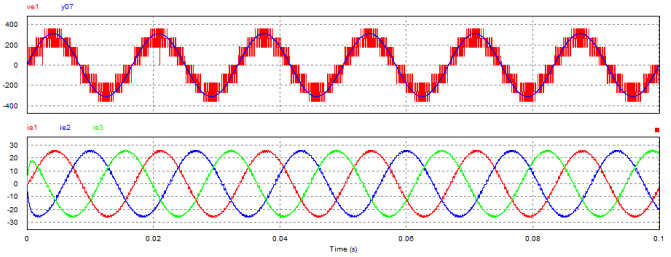

Fig. 6. Simulation results of the dual-inverter system output signal. Upper traces: phase voltage (red) and the voltage reference (blue). Bottom traces: three phase-currents.

V. Analysis of the Semiconductor Losses

In this section, a comparative analysis between the conventional and proposed PWM technique is realized, considering two operating scenarios, in terms of switching and conduction losses, and the total harmonic distortion (THD) level of current i_{e1} and voltage v_{e1}. To perform the simulations, the same kind of semiconductor devices were in both converters. In scenario 1, both the systems operated at the same switching of 3 kHz frequency, while in scenario 2 the current THD was fixed at close to 3%.

To find the value of 3%, simulations were realized by changing the value of the switching frequency until reach the required THD value. In this case, for the dual-inverter system, this frequency was 2.85 kHz and, for the conventional system,

was 6.25 kHz. The TABLE I and TABLE II summarize the results of conduction losses (P_D), switching losses (P_Q), total system losses (P_T) and THD levels, respectively, for scenarios 1 and 2.

TABLE I. SEMICONDUCTOR LOSSES AND THD LEVELS OF THE DUAL-INVERTER AND CONVENTIONAL SYSTEMS CONSIDERING THE SCENARIO 1.

	Dual Inverter	**Conventional Inverter**
Switching frequency	3 kHz	3 kHz
THD (i_{e1})	2.93%	6.2%
THD (v_{e1})	27.24%	52.58%
P_{Q1a}	7.23 W	27.53 W
P_{Q1b}	6.84 W	-
P_{D1a}	16.22 W	16.37 W
P_{D1b}	16.22 W	-
P_T	138.94 W	130.19 W

TABLE II. SEMICONDUCTOR LOSSES AND THD LEVELS OF THE DUAL-INVERTER AND CONVENTIONAL SYSTEMS CONSIDERING THE SCENARIO 2.

	Dual Inverter	**Conventional Inverter**
Switching frequency	2.85 kHz	6.25 kHz
THD (i_{e1})	3.08%	3%
THD (v_{e1})	27.26%	52.85%
P_{Q1a}	6.80 W	64.19 W
P_{Q1b}	6.82 W	-
P_{D1a}	16.25 W	16.29 W
P_{D1b}	16.25 W	-
P_T	137.53 W	241.24 W

As can be observed from the results of TABLE I, the dual-inverter system resulted in a current THD around 2.9%, that is, 47% lower than the current THD produced by the conventional system when was considered the same switching frequency of 3 kHz. This is because the dual-inverter system produces more voltage levels than the conventional, which can be verified by the THD-voltage values, i.e., 52% lower in the dual-inverter system in relation to conventional. For the semiconductor losses, switching losses in the dual-inverter system, specifically, in converters A and B were, respectively, 26.26% and 24.84% (about 51% in total) lower than in the conventional system, given that the applied voltage to the switches of converters A and B is the half required for the conventional converter.

On the other hand, as dual-inverter system is constituted of two series-connected converters, then, the current level is theoretically the same as conventional system. As a result, the conduction losses on the dual-inverter and conventional converters were practically equal. Therefore, the dual-inverter system produced approximately 6.29% more total losses than the conventional. Note that, in this scenario, although the dual-inverter system has twice number of semiconductor devices, the total losses are close to the conventional.

The results presented in TABLE II referred to scenario 2, in which the THD-current level was fixed at 3%, so that the switching frequency was adjusted at 2.85 kHz and 6.25 kHz for the dual-inverter and conventional systems, respectively. As can be verified, the values of THD voltage presented minor variations, since this mostly depends on the number of voltage levels. For the semiconductor losses, the switching losses in the dual-inverter system, considering the converters A and B, were around 10.6% (about 21% in total) lower than in the conventional system. Note that there was a significant reduction compared to the previous scenario. In addition, the conduction losses in this scenario remained as the current magnitude is the same for both scenarios. Therefore, total losses in the dual-inverter system were 57% lower compared to the conventional. This proves that the proposed PWM technique had provide to the dual-inverter system a more efficient operation than the conventional on the condition that it produces the same quality of current form.

VI. CONCLUSION

In this paper, the model of a dual-2L-inverter system was developed and from it a digital scalar PWM modulation technique was implemented by exploiting the degrees of freedom of the drive system. The theoretical analysis was validated by simulations, emulating a three-phase induction motor from a three-phase load. Moreover, carrier-based modulation techniques were studied and applied with the inclusion of zero-sequence apportionment factor μ_0 for conventional systems, which resulted in 5 output voltage levels. For the dual-inverter system, besides the inclusion of the factor μ_0, the differential pole voltage apportionment factor μ_j was defined, that allowed the generation of 9 voltage levels at the output. Given this, the dual-inverter system using the proposed PWM technique has presented more satisfactory results relative to the output waveform quality, considering that it is possible to produce low harmonic content in the current.

Since the dual-inverter system has twice the number of semiconductor devices compared to the conventional system, the losses on these devices were evaluated under two operating scenarios, considering: i) same switching frequency and ii) same THD-current level. From a comparative analysis, it was found that the proposed PWM technique has provided to the dual-inverter system a more efficient operation than the conventional in the second scenario, when both has presented the same current waveform quality. Note that the voltage applied on the semiconductor devices of the dual-inverter system is lower compared to the conventional system, which represents lower voltage efforts. In addition, the dual-inverter system has 64 switching states, so that losses can be minimized from the optimal selection of switching states.

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