# A Single-Phase Rectifier Using Zeta Converter in Discontinuous-Capacitor-Voltage Mode

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***Abstract*— This paper proposes a single-phase high power factor rectifier using a Zeta converter in discontinuous capacitor voltage mode (DCVM). In DCVM, the power converter input current is linearly dependent on its input voltage when the duty cycle is constant. Thus, the operation in DCVM allows the implementation of a rectifier with high power factor and low harmonic distortion. This work also includes a steady-state analysis and a design method for the proposed rectifier.**

***Keywords*— *High Power Factor Rectifier, PFC, DCVM, Zeta converter.***

## I. INTRODUCTION

The design of a high power factor rectifier (HPFR), also known as power factor corrector (PFC), usually contemplates the operation in three distinct conduction modes. These are the continuous inductor-current mode (CICM), the discontinuous inductor-current mode (DICM) and the boundary inductor-current mode (BICM) [1][2] where the power converter operates in the boundary between the CICM and the DICM.

According to [3-7] the power converters of the buck-boost family have the inherent ability to operate as ideal HPFRs, when operating in a discontinuous current inductor mode (DICM) with a fixed duty cycle [7]. However, the price paid for this feature is the high current stress in its switches, which increases the overall losses of the power converter.

The dual from DICM operation is the discontinuous capacitor-voltage mode (DCVM), and, as its name suggests, has the characteristic of presenting a time interval, in which the coupling capacitor (*C*) voltage waveform remains constant or null, i.e., its current is zero during this time interval. The DCVM presents some advantages, such as transistor turn-off soft switching, almost ideal power factor and low current stress in its semiconductors [2].

One of the greatest advantages of the DCVM is that the power converter can work as an HPFR without any complex control strategies. In order to achieve high power factor, it is sufficient to keep the duty cycle constant within the low-frequency period. Moreover, it also presents low current ripple on its inductors and an almost unity power factor [1][2].

G. Spiazzi et al reported the discontinuous capacitor voltage mode (DCVM) for a Ćuk based HPFR [1]. The operation in this mode allows the implementation of an almost ideal HPFR, with low input current ripple and high power factor. Unlike the operation in DICM, the operation in DCVM ensures that the currents in both inductors never become null, nor remain constant in any of the operation stages, analogous to what occurs when the converter operates in CICM. Nevertheless, maintaining the main advantage of the implementation of HPFRs in DICM, which is the ability to achieve unity power factor without the needing of duty-cycle modulation [1][2]. Unfortunately, the operation in DCVM causes high voltage stresses across the semiconductors, calling for high-voltage switches like IGBT's.

Although the first report of a Ćuk based HPFR in DCVM was in 1995 [1], this conduction mode remains under research [8-11] and its use with a Zeta based HPFR is narrowly described in the literature.

The Zeta converter shown in Fig. 1 presents itself as an attractive solution to implement HPFRs [12]. Once the converter has current source characteristics at its output, it is easy to obtain galvanic isolation by replacing the $L_m$ inductor by two magnetically coupled inductors. This topological change is analogous to the one that transforms the buck-boost converter in the Flyback converter. This ensures the desired electrical safety of the system. The Zeta converter also presents the possibility to obtain high PF, as well as reduced harmonic distortion, using input EMI filters.

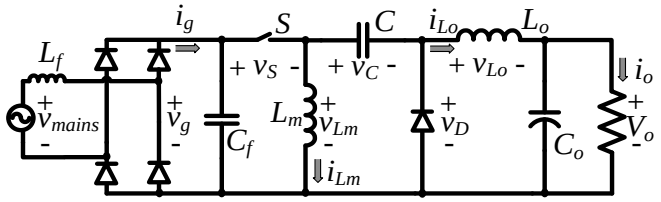


Fig. 1. Single-phase rectifier using zeta converter.

The paper includes a steady-state analysis and a simplified design method based on system linearization. A case study based on digital simulations is used to validate the proposed design criterion for achieving both a high PF and a low THD with a fixed duty cycle. Since the Zeta based HPFR in DCVM can operate in open loop, this study uses no control strategy. Nevertheless, for commercial use, the use of a voltage follower approach is the simplest solution for most of the applications.

The simulation results show that the operation in DCVM imposes lesser current stresses, but greater voltage stresses at the semiconductors.

## II. Steady State Analysis

### A. Operation Stages and Waveforms

This section shows a study of a single-phase rectifier using Zeta converter in discontinuous capacitor voltage mode (DCVM). Fig. 1 shows the power converter structure. Initially, this section presents the operation stages, the main waveforms, and main equations for the converter design.

The operation in DCVM leads to inductor currents that never become null as analogous to what occur in continuous inductor-current mode (CICM) [2]. However, keeping the duty cycle ($d$) constant in DCVM results in an input current that naturally follows the mains voltage, as in discontinuous inductor-current mode (DICM) [1][2]. The duty cycle in DCVM, just like in other conduction modes, is the ratio between the time in which the transistor is ON ($t_{on}$) and the switching period ($T$).

In DCVM there are three operation stages. In the first stage, the power of the mains flows through the switch $S$, while there is no current through the diode $D$. In the second stage, both semiconductors are simultaneously ON [1][2], keeping the coupling capacitor voltage ($C$) constant and, therefore, its current becomes null. Note that the diode turns on, in zero voltage switching (ZVS) condition. Finally, the third stage starts when the switch $S$ turns off, which occurs in ZVS condition, while the diode remains conducting. These three operation stages alternates at every switching period.

Fig. 2 shows that the first stage ($t_{S\,on}$) starts by the activation of the switch ($S$). The current flowing through the switch ($i_S$) is equal to the sum of the currents in the inductors $L_m$ ($i_{Lm}$) and $L_o$ ($i_{Lo}$). As the current $i_{Lo}$ flows through the coupling capacitor $C$ ($i_C$), the voltage at its terminals ($v_C$) grows positively until the point in which $v_C$ equals the Zeta converter input voltage ($v_g$). In this instant, the diode $D$ is directly biased and its current ($i_D$) is equal to the current $i_{Lo}$, resulting in the end of this stage.

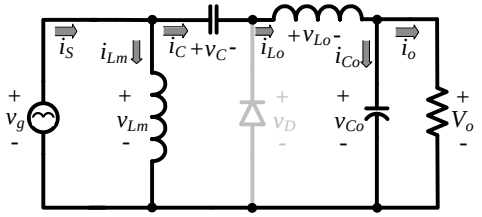


Fig. 2. First stage, when the switch $S$ is ON.

Fig. 3 shows the second stage ($t_{on}$-$t_{D\,on}$) in which the diode turns on, in ZVS condition. The output current flows through the diode, i.e., the current through the inductor $L_o$ ($i_{Lo}$). The switch $S$ remains activated, conducting the current $i_{Lm}$. This stage remains stable until the instant when the switch turns off.

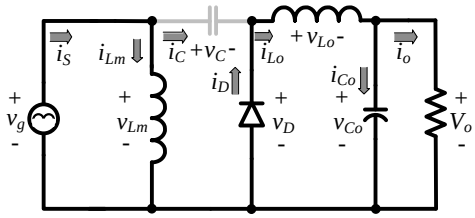


Fig. 3. Second stage, when both semiconductors are ON.

Fig. 4 presents the third stage ($t_{off}$) which begins when the switch ($S$) turns off in ZVS condition, the currents in the inductors $L_m$ and $L_o$ flow through the diode $D$. The capacitor $C$ discharges itself at this stage, which ends when the switch $S$ turns on again.

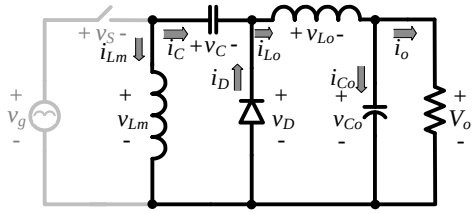


Fig. 4. Third stage, when the diode $D$ is ON.

Fig. 5 shows the main waveforms for a single-phase rectifier using Zeta converter in DCVM considering a switching period (SP). Therefore, the waveforms shown in this figure correspond to the currents $i_{Lm}$, $i_C$, $i_{Lo}$, $i_S$ and $i_D$; and the voltages on the capacitor $C$ ($v_C$), on the inductor $L_m$, ($v_{Lm}$), on the inductor $L_o$ ($v_{Lo}$), on the switch $S$ ($v_S$) and on the diode $D$ ($v_D$).

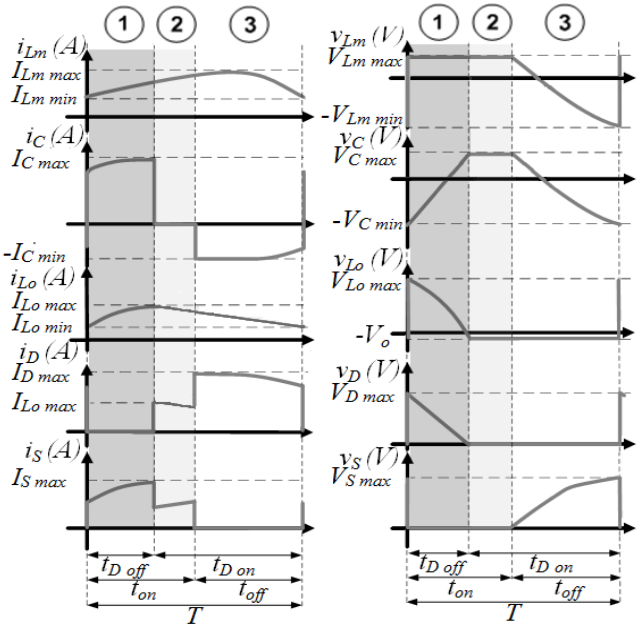


Fig. 5. Main waveforms for a Zeta converter in DCVM in a SP.

Fig. 5 shows that the currents on the inductors never become null, which is a feature proper of the operation in CICM.

Observing Fig. 5 it is remarkable that in the second operation stage the capacitor current and voltage curves present a discontinuity, which gives the name for this operation mode, since at this operation stage the capacitor voltage remains constant and its current is zero.

### *B. Design Guidelines*

This section offers a practical guideline, based on [13], for designers interested in using a Zeta based HPFR in DCVM. The proposed design criterion consists of a set of design equations associated to a set of design restrictions, such as, the rated values of the output power ($P$), output voltage ($V_o$), switching frequency ($f_s$), mains rms voltage ($V_{g\,rms}$) and mains peak voltage ($V_g$).

As the bigger the inductance $L_o$ is, the smaller will be its current ripple and consequently, the smaller will be the HPFR output current ripple. Therefore, the rated output inductance is a function of the square of the voltage $V_o$, the power ($P$) and the switching frequency ($f_s$). This relation is

$$L_o \le \frac{4.4\,V_o^2}{P\,f_s}, \tag{1}$$

A significant difference between the DCVM and the DICM is that in DICM the coupling capacitor $C$ must have a capacitance high enough to keep the voltage on its terminals almost constant within a switching period. On the other hand, in the DCVM, the capacitance of capacitor $C$ must be low enough to allow the voltage on its terminals to vary between a negative minimum value and a positive maximum value, respectively ($-V_{C\,min}$) and ($V_{C\,\max}$) within a switching period ($\Delta v_{C\,max}$). In the second stage, it does not vary, creating a discontinuity. Considering a mains voltage drop of 30 % due to the input filter, it results in a capacitor

$$C = \frac{G^2}{6\,f_s\,R\left(G^2+2\,G+1\right)}. \tag{2}$$

where $G$ is the static voltage gain of the converter, ($G = 1.3 \times V_o/V_{g\,rms}$ because of the input filter losses). The following component designs ignore these losses to avoid the use of unnecessary bigger components.

The duty cycle ($d$) of the Zeta based HPFR working in DCVM is a function of the time constant ($R\,C$), of the switching frequency ($f_s$) and of the voltage gain ($G$), as follows

$$d \approx 1 - \frac{\sqrt{2\,R\,C\,f_s}}{G}, \tag{3}$$

where $R$ represents the output load.

In addition to the above mentioned parameters, the power converter output voltage ($V_o$) depends on the duty cycle ($d$) and on the rms value of the mains voltage ($V_{g\,rms}$), resulting in

$$V_o = V_{g_{\,rms}}\sqrt{1.18\,\frac{R\,C\,f_s}{1-d}}, \tag{4}$$

Nevertheless, the inductance $L_m$ determination is possible through a function of the duty cycle, the peak voltage, switching frequency and the current ripple ($\Delta i_{Lm}$). The equation (5) assumes that this ripple is twice the rms value of the current at this inductor.

$$L_m = \frac{\sqrt{2}V_g^2\,d}{4\,f_s\,P}. \tag{5}$$

The output capacitor ($C_o$) aims to minimize the low-frequency ripple, of the output voltage ($\Delta v_o$), which is intrinsic to most HPFRs. The ripple $\Delta v_o$ for this design should be a fourth of the output voltage ($\Delta v_o = V_o/4$). Moreover, the rated capacitance of the output capacitor comes from the fundamental component of the ac current that flows through the capacitor, resulting in

$$C_o = \frac{0.18\,P}{V_o\,\Delta v_o\,f_{mains}}, \tag{6}$$

where $f_{mains}$ is the mains frequency. This equation comes from the fundamental component of the ac current that flows through the capacitor.

Finally, the design of the EMI input filter formed by the inductor $C_f$ and the capacitor $L_f$. The filter capacitor manipulates the power at the load. Multiplying the equation $E = (½)\,C_f\,V_g^2$ in both sides by the switching frequency; and isolating the capacitance $C_f$ results in

$$C_f \le \frac{2\,P}{V_g^{\,2}\,f_s}. \tag{7}$$

For the inductor design of the input filter, the resonant circuit frequency is about one decade below $f_s$, resulting in

$$L_f \le \frac{1}{2C_f\,f_s^2}. \tag{8}$$

## III. RESULTS

The results presented here comes from digital simulations of a Zeta based HPFR working in DCVM sized using the design methodology proposed in this paper and the power converter rated specifications, shown in Table I.

From (3) the rated duty cycle ($d$) is $d = 0.604$, ensuring a reasonable operating range, since both the power grid voltage and the load can vary. Table II shows the Zeta converter passive components sized according to the proposed design strategy and the power converter rated specifications shown in Table I.

TABLE I. DESIGN PARAMETERS

| Parameters | Values |
|---|---|
| $V_{in}$ | 127 V |
| $f_{mains}$ | 60 Hz |
| $f_s$ | 45 kHz |
| $P$ | 200 W |
| $V_o$ | 45 V |
| $I_o$ | 4.44 A |

TABLE II. ZETA CONVERTER IN DCVM - CAPACITORS AND INDUCTORS VALUES.

| Inductances | | Capacitances | |
|---|---|---|---|
| $L_f$ ($\mu H$) | 900 | $C_f$ ($nF$) | 274 |
| $L_m$ ($\mu H$) | 769.3 | $C$ ($nF$) | 36.27 |
| $L_o$ ($\mu H$) | 990 | $C_o$ ($\mu F$) | 1185 |

Figures 6 and 7 showing simulation results for full load. Fig. 6 presents the mains voltage and input current for a Zeta based HPFR working in DCVM with fixed duty cycle. The input current rms value is 1.77 A, its total harmonic distortion is 3.53 %, and the simulated power factor is 0.9993, almost unitary. Therefore, it is fair to say that the Zeta converter working in DCVM with fixed duty cycle has the ability to emulate a resistive load.

Figure 7 shows both the output voltage and the output current considering a resistive load. Therefore, from that figure one can observe that the average output current is a bit more than 4.7 A and the average output voltage is about 47.7 V, as designed. The simulation results showed that the proposed design methodology results in a minor, power converter oversizing (average $V_o$ at 47 V instead of 45 V), this feature probably would produce better results in a real prototype, where losses are present.

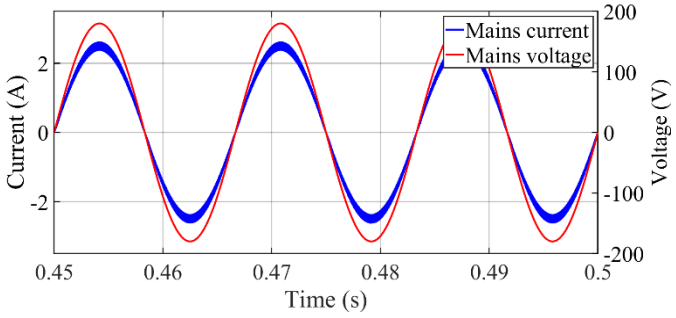


Fig. 6. Current and voltage input waveforms at mains period, for Zeta converter working in DCVM.

Output voltage ripple (Fig. 7) stays within the proposed level of one fourth of the output average voltage, and the oscillation frequency are double the mains frequency, once Flyback family HPFRs have a strong ac harmonic component on its output, 120 Hz in this case.

From these results, it is possible to establish that the Zeta based HPFR working in DCVM, in open loop with fixed duty cycle, present a good behavior as a resistive load from the mains point of view.

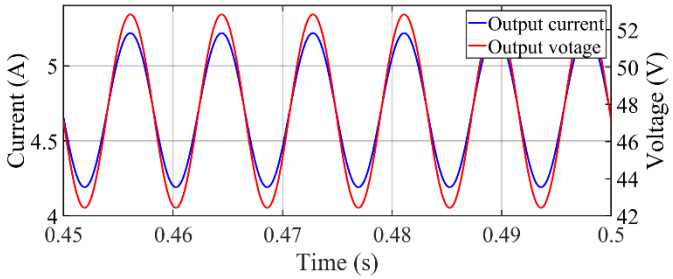


Fig. 7. Current and voltage output waveforms at mains period, for Zeta converter working in DCVM.

Fig. 8 presents the waveforms of the currents flowing through the capacitor $C$, as well as its voltage waveforms at mains and switching period. It is possible to verify that not only voltage waveforms in the capacitor are not continuous, as expected (because of the name of the converter operating mode), but also the current waveform. Therefore, the current and voltage ripples have both positive and negative parts. The peak current in the capacitor is around 9 A, and the peak voltage is around 550 V.

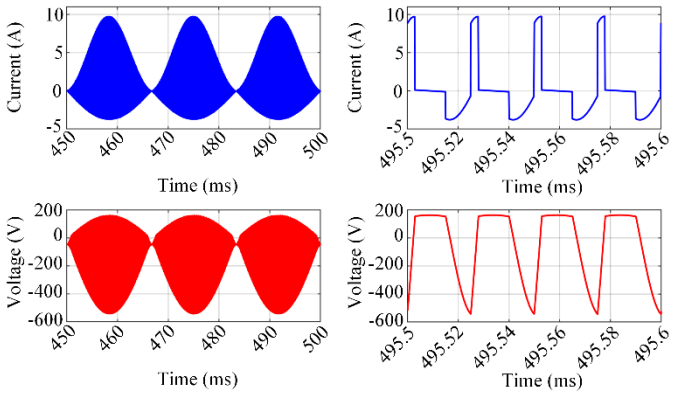


Fig. 8. Waveforms of the current and voltage in the capacitor $C$ at mains frequency (left figures) and switching frequency (right figures).

Fig. 9 depicts the waveforms of the current flowing through the switch $S$ ($i_S$) and the voltage across it, at mains and at switching period. It is verifiable that the transistor turns off at ZVS. The peak voltage stress in this semiconductor is almost 800 V, whereas the peak current is about 11.5 A.

Fig. 10 shows the waveforms of the current flowing through the diode ($i_D$) and the voltage across it, at mains and switching period. It is possible to see that the diode turns on in ZVS. It is clear to see that the current flows through the diode in two switching stages, though with different intensities. The diode is at maximum current stress (~ 13 A) only at the start of the third stage, while the maximum voltage stress (almost 800 V) occur at the very start of the first period.

Fig. 11 presents the waveforms of the current flowing through the inductor $L_m$, as well as the voltage waveforms across this inductor, at mains and switching period. The current ripple in the inductor $L_m$ is about 3.1 A. The maximum value of this current reaches almost 4 A. The maximum voltage stress reaches about 500 V.

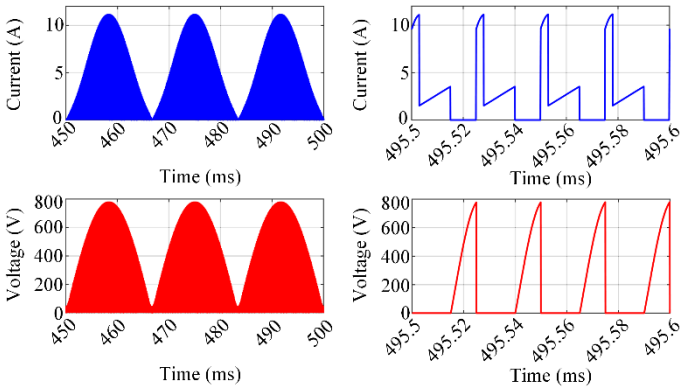


Fig. 9. Waveforms of the current and voltage in the transistor $S$ at mains frequency (left figures) and switching frequency (right figures).

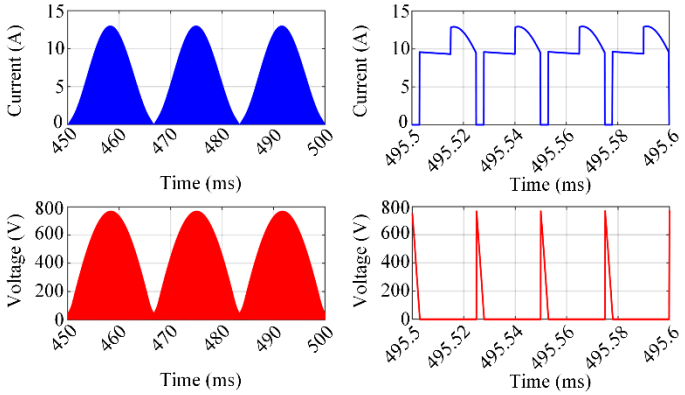


Fig. 10. Waveforms of the current and voltage in the diode $D$ at mains frequency (left figures) and switching frequency (right figures).

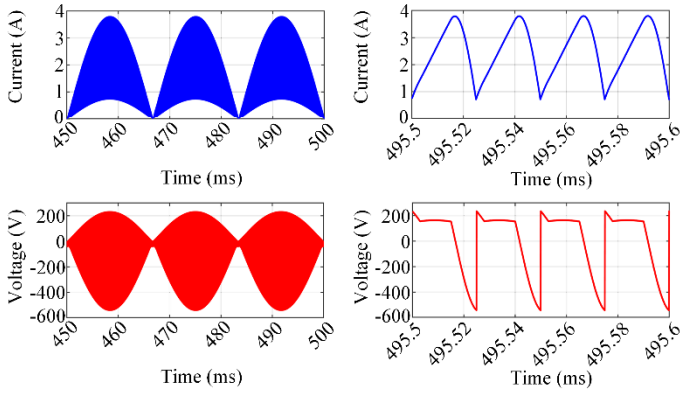


Fig. 11. Waveforms of the current and voltage in the inductor $L_m$ at mains frequency (left figures) and switching frequency (right figures).

Fig. 12 presents the waveforms of the current flowing through the inductor $L_o$, as well as the voltage waveforms across this inductor, considering the mains frequency and the switching frequency. It is clear that the current ripple in the inductor $L_o$ is much narrower than the current ripple in the inductor $L_m$, because of the design method. The current ripple is around 1 A, the peak current is about 10 A, while the peak voltage is about 700 V.

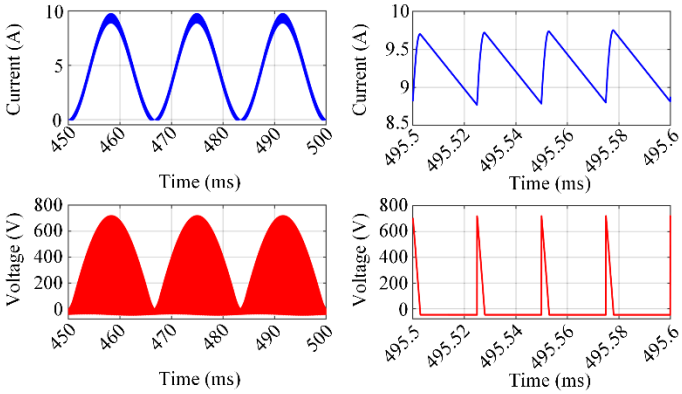


Fig. 12. Waveforms of the current and voltage in the inductor $L_o$ at mains frequency (left figures) and switching frequency (right figures).

Observing Fig. 11 and Fig. 12, it is evident that the current on each inductor only becomes null, when the mains voltage crosses zero, as occurs when the converter works in CICM. Fig. 13 presents the sum of the currents in the switch $S$ and in the diode $D$, in order to confirm that the HPFR in DCVM, with constant duty cycle, presenting an analogous behavior to that obtained in Zeta power converter in CICM.

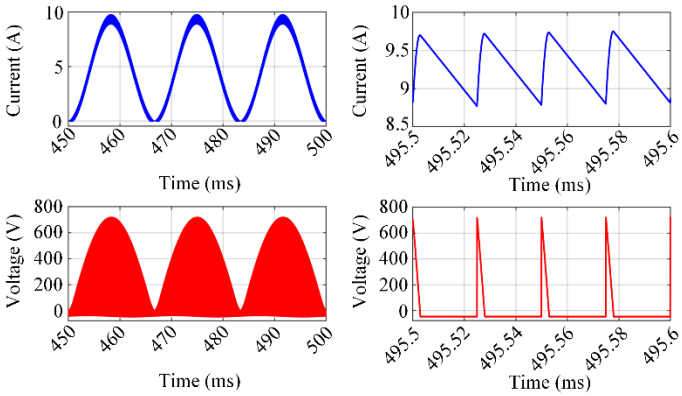


Fig. 13. Waveforms of the sum currents and sum voltages in the diode $D$ and in the switch $S$ at mains frequency (left figures) and switching frequency (right figures).

## IV. Conclusion

This paper investigated the use of the Zeta power converter working in discontinuous capacitor voltage mode (DCVM) to implement a high power factor rectifier (HPFR). In order to achieve this goal, the paper presents a steady state analysis for this HPFR and a design criterion. Ideal HPFRs can be implemented using Zeta, SEPIC or Ćuk converters working in

DICM [7], with constant duty cycle. However, almost ideal HPFRs can be implemented using Zeta, SEPIC or Ćuk converters working in DCVM, but with lower current stress on their semiconductors. Another substantial advantage of the DCVM is the considerable reduction of the coupling capacitor (*C*) capacitance in relation to the one necessary for the operation in DICM. It is enough keeping constant the converter duty cycle for implement almost ideal HPFRs with this conduction mode. The diode turn on and the transistor turn off are under ZVS commutation, which reduces the switching power losses and allows the power converter operation at higher switching frequencies.

On the other hand, one disadvantage of the HPFRs based on the Zeta converter working in DCVM consist in the increase of the voltage stress on the semiconductors. In addition, there is the fact that the rated values of its inductors are bigger than the ones required for a HPFR operating in DICM.

Therefore, this study indicates that the DCVM fits high current and low voltage applications, whereas the DICM is more suitable to an inverse scenario. One possible application for the DCVM is to implement LED drivers.

Evidently, the operation of Zeta based HPFR in CICM also allows the reduction of stresses in the semiconductors, whereas employing, practically, the same inductors used in the Zeta based HPFR designed for operating in DCVM. Moreover, the voltage and current stresses in the semiconductors in DCVM are greater than in CICM. However, the operation in CICM requires the use of a more complex control strategy, such as the average current mode control.

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