Use of a Boost-Forward DC-DC Voltage Source to Feed a Four-Level Flying Capacitor Inverter

Antonio Venâncio de M. Lacerda Filho*, Ronnan de B. Cardoso*, Edison R. C. da Silva*†
Andre E. L. da Costa† and Darlan A. Fernandes*
*Post-Graduate Program in Electrical Engineering – PPGEE – LOSE – CEAR
Federal University of Paraíba – UFPB, João Pessoa – PB, Brazil
†Post-Graduate Program in Electrical Engineering – PPGEE – COPELE – LEIAM
Federal University of Campina Grande, UFCG – PB, Brazil
e-mail: antonio.lacerda@cear.ufpb.br, ronnan.cardoso@cear.ufpb.br, ercdasilva@gmail.com
andre.lucenadacosta@gmail.com, darlan@cear.ufpb.br

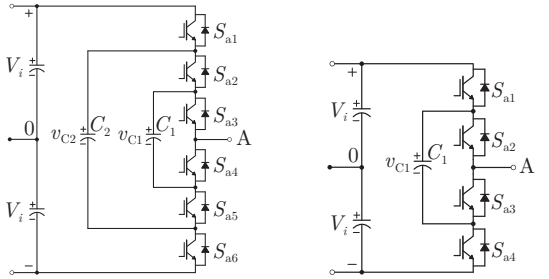
***Abstract*—This paper investigates the possibility of operation of four-level flying capacitor inverter obtained from a three-level flying capacitor structure in which the flying capacitor is replaced by a boost/forward DC-DC voltage source of adequate fixed value. The regulation of the flying capacitor is easily obtained in open loop without any complicated PWM strategy. Also, the theoretical studies are validated by simulated and experimental results. Comparative studies show that the solution is not so advantageous for the four level structure.**

***Keywords* – Multi-level inverter, four-level inverter, flying capacitor inverter, DC-DC converter-fed inverter, DC-DC hybrid converter.**

I. Introduction

The most well known multilevel topologies are the Full-Bridge Cascade (FBC) [1], [2], the Neutral Point Clamped (NPC) [3], [4], and the Floating Capacitor (FC) [5], [6] ones. While the H-bridge allows for obtaining three levels, the most basic FBC is constituted by two cascaded full-bridges (eight switches) individually fed by isolated sources providing five levels (5L). In case of NPC and FC, higher level topologies can be obtained as an extension of the well-known three-level ones. The conventional four-level (4L) structures for FC and NPC employ six main power switches. In case of NPC six additional clamping diodes (considering that they are cascaded to block higher voltage); similar, in case of FC three additional capacitors are requested (considering that they are cascaded to block higher voltage, and excluding those of the DC-bus). This not only increases cost but also the control complexity for regulating the voltages of either the NPC DC-bus capacitors or the FC DC-bus capacitors and flying capacitors.

Figure 1(a) shows the single-phase four-level conventional FC (4L-CFC) topology, in which the DC-bus voltage is $2V_i$ while the capacitor voltages are $2V_i/3$ and $V_i/2$. However, the number of flying capacitors may be reduced by adequate regulation of the capacitor voltage value in the three-level structure shown in Fig. 1(b) [7]. Table I indicates its possible states of operation as a function of the floating capacitor voltage v_{C1}. It can be seen that when the value of the floating capacitor voltage is different from V_i, four levels are obtained.



(a) Three-cell FC topology (b) Two-cell FC topology

Fig. 1. 4L-FC inverters.

TABLE I
State of operation.

State	S_{a1}	S_{a2}	S_{a3}	S_{a4}	v_{A0}	v_{C1}=$\frac{V_i}{2}$	v_{C1}=$\frac{V_i}{3}$
1	1	1	0	0	V_i	V_i	V_i
2	1	0	1	0	V_i-v_{C1}	$V_i/2$	$V_i/3$
3	0	1	0	1	-V_i+v_{C1}	-$V_i/2$	-$V_i/3$
4	0	0	1	1	-V_i	-V_i	-V_i

Considering that $2V_i$ is the DC-link voltage, the specific cases $v_{C1} = V_i/2$ and $v_{C1} = V_i/3$ are indicated in both Table I and Fig. 1(b). The capacitor voltages regulation in Fig. 1(a) are obtained by PWM control [8]. However, in order to avoid PWM control complexity it is possible to use a fixed DC-source or a DC-DC converter instead of a capacitor C_1 in Fig. 1(b) [7].

On the other hand, there are different voltage DC-DC converter topologies that can step-up the voltage generate by sources as PV arrays [9], [10], [11]. Some of them have been used to supply inverters as shown in [12] and [13]. In this regard, an interesting issue applied to FC inverters is the use of the combined boost/flyback converter topology introduced in [14]. In that topology, two isolated voltage outputs are available: step-up for feeding the DC-bus; and step-down for regulating the voltage value of the floating capacitor. However, high gain can be also obtained from the combined boost/forward converter [15].

This paper investigates the possibility of obtaining a four

level inverter topology with the help of such a step-up voltage gain DC-DC boost-forward converter with dual output using single power stage that imposes a fixed flying capacitor voltage. Regulation of this floating source is easily obtained without any complicated PWM strategy. In order to see the feasibility of its application it is compared to the four-level conventional FC inverter with the capacitor voltages regulated with PWM.

The paper is organized as follows: Section II describes operating principles of the proposed four-level combined converter; Section III discusses its modulation strategy and provides design considerations for the topology; Section IV gives the simulation verification; Section V presents the experimental results; in Section VI comments are given; finally conclusion is presented in Section VII.

II. The Proposed Four-Level Combined Converter

The use of a DC-DC boost-forward converter (BFdC) to feed the flying capacitor results in the proposed converter in Fig 2. The boost-forward (BF) part of the proposed converter was idealized from the union of a rearranged buck-boost converter [16] and a forward converter. As shown in Fig 2, such arrangement evidences the utilization of voltage $v_o = V_i + v_{C2}$ as DC-link voltage while providing a neutral point access. This part is constituted of three diodes, D, D_1 and D_2, three switches, S, S_1 and S_2, a high-frequency transformer and two output capacitors, C_1 and C_2. Switches connected in anti-parallel with diodes D_1 and D_2 guarantee the floating capacitor voltage regulation at the desired value.

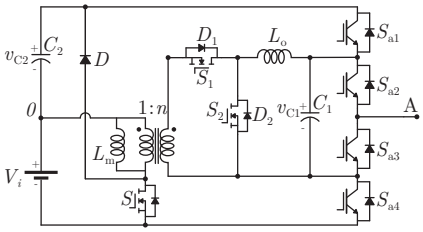


Fig. 2. Proposed combined 4L-BFd-FC converter.

The operation frequency of the BFdC is higher than that of the power inverter itself. When considered in separate that converter has two modes of operation: one when switch S is *on* (*Mode A*) and the other when it is *off* (*Mode B*). Then for each operation state of the inverter, as indicated in Table I, two modes of the DC-DC converter do occur. As a result there are sixteen modes of operation for the combined converter. However, only eight of them, corresponding to the positive load current half-cycle, are presented in Fig. 3 and Table II.

A. Considerations on the Boost-Forward Converter

Before considering these eight modes of Table II, a description of the two DC-DC converter modes will be given. *Mode A* is shown in figures 3(a), 3(c), 3(e) and 3(g), while *Mode B*, is shown in figures 3(b), 3(d), 3(f) and 3(h). In the following description, the coupled inductor is modeled as an ideal transformer, which consists of a turn ratio of $1/n$ and a

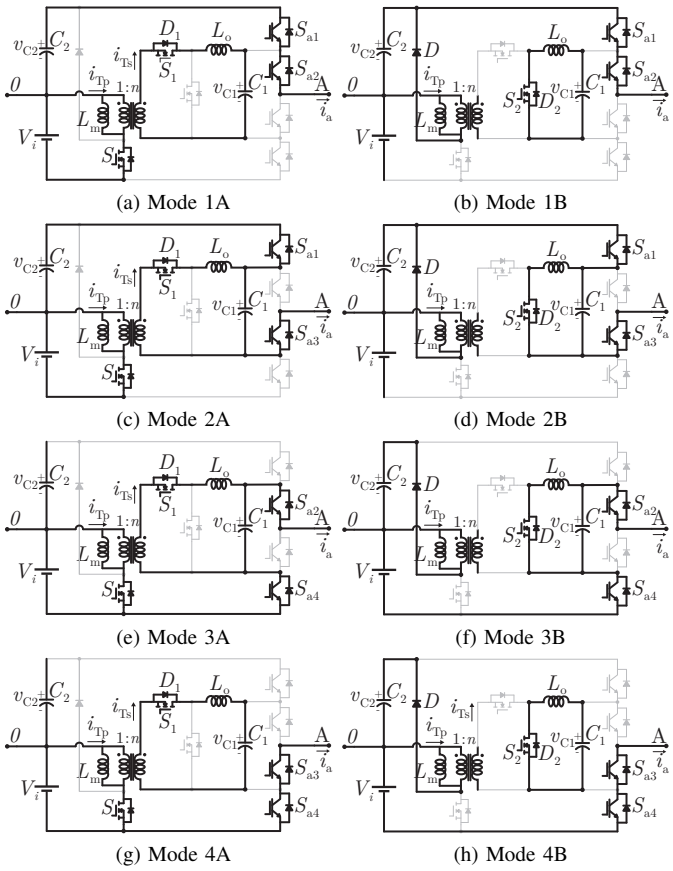


Fig. 3. Modes of operation of the 4L-BFd-FC.

TABLE II
Modes of Operation.

	DC-DC Converter				Inverter				
State	S	D	S_1	S_2	S_{a1}	S_{a2}	S_{a3}	S_{a4}	v_{A0}
1A	1	0	1	0	1	1	0	0	V_i
1B	0	1	0	1	1	1	0	0	V_i
2A	1	0	1	0	1	0	1	0	V_i-v_{C1}
2B	0	1	0	1	1	0	1	0	V_i-v_{C1}
3A	1	0	1	0	0	1	0	1	-V_i+v_{C1}
3b	0	1	0	1	0	1	0	1	-V_i+v_{C1}
4A	1	0	1	0	0	0	1	1	-V_i
4B	0	1	0	1	0	0	1	1	-V_i

magnetizing inductor L_m. It is considered that its operation, and also that of the output inductor filter, is in the continuous mode (CCM). In addition, all components are considered to be ideal. The typical waveforms of the DC-DC converter are illustrated in Fig. 4, for CCM operation and positive i_{Lo} current.

- *Mode A* $[0 < t < DT_s]$

This mode is shown in the DC-DC converter part of Fig. 3(a), for instance. At instant t_0 switch S is turned *on* and energy is transferred to the transformer secondary from the voltage source. During this time interval diodes D and D_2 are reverse-biased, diode D_1 is *on* and switch S_1 is turned *on*. Conduction of either D_1 or S_1 depends on the condition of

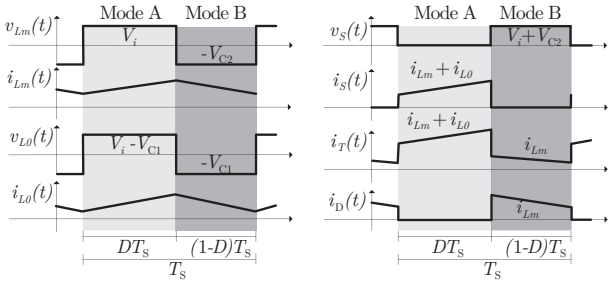


Fig. 4. Typical waveforms of the DC-DC converter

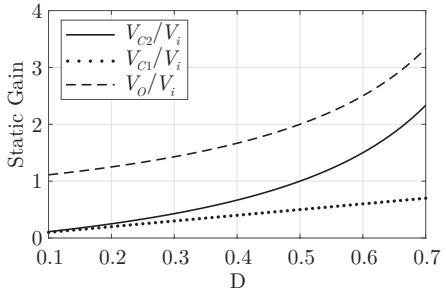


Fig. 5. Converter static gains.

capacitor C_1 that, in turn, also depends on the inverter modes. At the same time the magnetizing current increases (see Fig. 4) and reaches its peak value at instant DT_s. Same for i_S and for the secondary current, i_{Ts}. Capacitor C_2 together with the voltage source V_i supplies energy to the DC-link. Equations for *Mode A*, are:

$$\frac{di_{Lm}}{dt} = \frac{V_i}{L_m} \qquad \frac{di_{Lo}}{dt} = \frac{nV_i - V_{C1}}{L_o} \tag{1}$$
$$\frac{dV_{C1}}{dt} = \frac{i_{Lo} - i_a}{C_1} \qquad \frac{dV_{C2}}{dt} = \frac{-i_a}{C_2}$$

In these equations i_a is the phase current. It will be seen that in certain modes the load current will not circulate in the capacitor. In these cases, current i_a is eliminated from the equation to calculate v_{C1}.

- Mode B $[DT_s < t < T_s]$

At instant DT_s, switch S is turned *off* and diodes D and D_2 or S_2 start to conduct. The equivalent circuit is shown in part of Fig. 3(b). In this interval the currents in inductors L_m and L_o decrease. The current in L_o flows through D_2 (S_2) and charges (discharges) capacitor C_1. Capacitor C_2 charges with the energy transferred from L_m. Equations for this interval are:

$$\frac{di_{Lm}}{dt} = \frac{-V_i}{L_m} \qquad \frac{di_{Lo}}{dt} = \frac{-V_{C1}}{L_o} \tag{2}$$
$$\frac{dV_{C1}}{dt} = \frac{i_{Lo} - i_a}{C_1} \qquad \frac{dV_{C2}}{dt} = \frac{i_{Lm} - i_a}{C_2}$$

There are modes the load current will not circulate in the capacitor. In these cases, current i_a is eliminated from the equation to calculate v_{C1}.

In fact, in these modes current i_{Lo} can be either positive (with D_1 conducting) or negative (with S_1 conducting), depending on the current imposed by the inverter.

The static gain is obtained through the energy balance in the magnetizing inductance with the help of Fig. 4. That is,

$$\frac{V_{C2}}{V_i} = \frac{D}{(1-D)}; \quad \frac{V_{C1}}{V_i} = nD; \quad \frac{V_o}{V_i} = \frac{1}{(1-D)} \tag{3}$$

The gain corresponding to (3) is depicted in Fig. 5 when $n = 1$.

For $D = 0.5$, the DC-bus voltage is $2V_i$ and the flying capacitor voltage is $V_i/2$. These conditions are maintained for $D = 0.5$ even when winding resistances r_{e1} and r_{e2} in the coupled inductor, on-state equivalent resistances r_{e1} and r_{e2} of paralleled diodes D_1/S_1 and D_2/S_2, and on-state resistance $r_{DS}(on)$ of the power switch are considered.

B. Modes of Operation of the Combined Converter

It has been shown above that operation of the DC-DC converter with $D = 0.5$ and $n = 1$ allows conditions so that the inverter can deliver four-level voltage at the phase output. The flow of energy in the DC-DC converter, that is, the conduction of D_1, S_1, D_2, and S_2 is mostly defined by *Modes 2A*, *2B*, *3A* and *3B*. Operation modes of the integrated converter will be now described.

Mode 1A – In this mode S, S_{a1} and S_{a2} are conducting (S_{a3} and S_{a4} are *off*) while the transformer secondary transfers energy from the voltage source. As in *Mode A*, diodes D_2 and D are reverse-biased, diode D_1 is *on* and S_2 is *off*. The voltage applied to the phase output is $V_{C2} = +V_i$. Capacitor C_1 can be considered to be approximately with voltage $V_i/2$.

Mode 1B – S_{a1} and S_{a2} continue conducting but S is turned *off* and diodes D_2 and D start to conduct. As in *Mode B*, switch S_2 is turned *on* in synchronism with S opening. Conduction of either D_2 or S_2 depends on the direction of the current in L_o. The energy stored in the magnetizing inductance at the end of the first mode is transferred to capacitors C_2. The phase output is also $V_{C2} = +V_i$. In this interval the energy in L_o charges C_1. S_2 and S_1 in next mode help to regulate the voltage.

Mode 2A – During this stage S_{a2} is turned *off*, S_{a1} continues conducting and S_{a3} is turned *on*. S is conducting and so is the transformer secondary. Behavior of the DC-DC converter is the same as in *Mode A*. The ideal voltage applied to the phase output is $V_{C2} = +V_i - V_i/2 = +V_i/2$. In this mode the capacitor current is composed by current i_a, circulating via S_{a1}, and by current i_{Lo}. Conduction of S_1 helps the capacitor voltage regulation so that the secondary current i_{Ts} can circulate by either D_1 or S_1. This depends on the direction of current i_{Lo}.

Mode 2B – In this mode, S_{a2} continues to be *off* while S_{a3} is *on*, as in *Mode 2A*, but S is turned *off*. Operation of the BFdC is as in *Mode B*. The phase output is also $+V_i/2$. In this interval the capacitor voltage regulation is obtained grace to S_2. Depending on its direction current i_{Lo} can circulate by either D_2 or S_2.

Mode 3A – In this mode S_{a3} is turned *off*, S_{a4} continues conducting after S_{a2} is turned *on*. S is conducting and so

is the transformer secondary. Diodes D_2 and D are reverse-biased and switch S_2 is *off* as in *Mode A*. The voltage applied to the phase output is $V_{C2} = -V_i + V_i/2 = -V_i/2$. Discussion on the current i_{Lo} behavior is similar to that in *Mode 2A*.

Mode 3B – As in *Mode 3A*, S_{a3} is *off*, and S_{a4} and S_{a2} are *on* but S is turned *off*. As in *Mode 1B*, the energy stored in the magnetizing inductance at the end of the first mode is transferred to capacitor C_1 via diode D_1, which is turned *on*, and to capacitor C_2 via D. Phase output is also $-V_i/2$. Discussion on current i_{Lo} behavior is similar to that in *Mode 2B*.

Mode 4A – During this interval, S_{a1} and S_{a2} are *off* while S_{a3} continues to be *on* and S_{a4} is turned *on*. As in *Mode 1B* S is *on* while D_1 is conducting and S_1 turned *on*. The transformer is energized and the voltage applied to the phase output is $-V_i$.

Mode 4B – During this stage, the inverter operates as in *Mode 4A*, that is, S_{a1} are S_{a2} *off*, S_{a3} and S_{a4} are *on*, S is *off* while D_2 is conducting and S_2 turned *on*, as in *Mode 1B*. Phase output is also $-V_i$.

C. Design Methodology

The value of D is chosen from Fig. 5 and the load current, secondary filter inductor current and magnetizing current are calculated from power specification. Inductances and capacitances are calculated from respective voltage ripple and current specifications. For instance, the flying capacitance can be calculated as a function of the peak current and the voltage variation from [17].

$$C_1 = \frac{I_{pk}}{2\,\Delta V_{C1}\,f_s\,m} \tag{4}$$

in which I_{pk} is the peak current and m is the modulation index. Semiconductors are specified from *rms* and average values.

III. Modulation Strategy

The pulse pattern, as shown in Fig. 6, can be obtained from a carrier-based PWM strategy for $v_{C1} = V_i/2$.

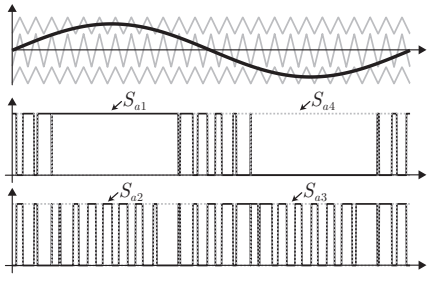


Fig. 6. Pulse pattern.

Three triangular carriers are level-shifted in-phase disposition (IPD PWM). Intersection of the modulating signal with each of the carriers from the top to the bottom generates pulses to S_{a1}, S_{a4}, S_{a2} and S_{a3}. It is worth mentioning that switches S_{a1} is complementary to S_{a4} and S_{a2} to S_{a3}. Regulation of v_{C1} around $V_i/2$ is obtained by maintaining the duty cycle of switch S at $D = 0.5$. For relation 1:3 the carriers in Fig. 6 have all the same amplitude.

IV. Simulation Results

The topology of Fig. 2 was simulated with the help of PSIM for voltages $V_{C1} = 75$ V and a DC-bus voltage $V_0 = 300$ V, from a DC voltage source, V_i, of 150 V. A duty cycle $D = 0.5$ was employed in the DC-DC converter what allows continuous conduction mode of operation. In order to reduce the transformer volume, the converter was operated at 40 kHz. A R-L circuit composed the load: R_{load} = 16 Ω; L_{load} = 7 mH. Design specifications and parameters are given in Table III and Table IV.

TABLE III
Design Specification.

Specification	Symbol	Value
Ouput power of output 1	P_{01}	290 W
Inverter ouput power	P_0	450 W
Current ripple in L_m	Δi_{Lm}	$0.1 i_{Lm}$
Current ripple in L_o	Δi_{Lo}	$0.1 i_{L0}$
Maximal voltage ripple in C_1	ΔV_{C1}	$0.0125 V_{C1}$
Maximal voltage ripple in C_2	ΔV_{C2}	$0.0125 V_{C2}$
DC converter Modulation frequency	f_s	40 kHz
Duty-cycle	D	0.5
Inverter modulation frequency	f_0	10 kHz

TABLE IV
Converter Parameters.

Specification	Symbol	Value
Winding ratio 1	n	1
Magnetizing inductance	L_m	4.3 mH
Output filter inductance	L_o	2 mH
Floating capacitance	C_1	2200 μF
DC-bus capacitance	C_2	2200 μF
Load resistance	R_{Load}	16 Ω
Load inductance	L_{Load}	7 mH

Figure 7 shows the output voltage (top) and load current (bottom). Better THD results can be obtained when $v_{C1} = 1/6 V_i$. Figure 8 show different variables for operation in the sequence of *Modes 1A*, *1B*, *2A* and *2B*. From the top to the bottom: voltage v_{A0} is presented at the top (between 76 V and 150 V); next there is a detail of current i_{Sa1} ripple and the current through S_{a3} (both around 7 A); then it is seen the current flowing through switch S with a small peak value at the end of the interval (0.8 A); in the following is presented the capacitor C_2 voltage, which is fed by the current of diode D_1; in the succeeding figures it can be seen that the current in inductor L_o is negative what imposes conduction of switches S_1 and S_2; finally it is shown that capacitor C_1 voltage, v_{C1}, is charged every time S_{a2} is turned *off*. Note that the current in D is resultant from the energy stored due to i_S and i_{S1}. Other intervals have similar behavior except in reactive intervals in which diodes D_1 and D_2 conducts instead of switches S_1 and S_2. Figure 9 shows an interval in which the currents of the the transformer secondary, i_{Ts}, flows through either diode D_1, i_{D1}, or switch S_1, i_{S1}, thus affecting the transformer primary current, i_{Tp}. It can be seen from Fig. 10 that voltages V_{C1} e V_0 reach the expected values of 75 V and 300 V, respectively, for an input voltage of 150 V.

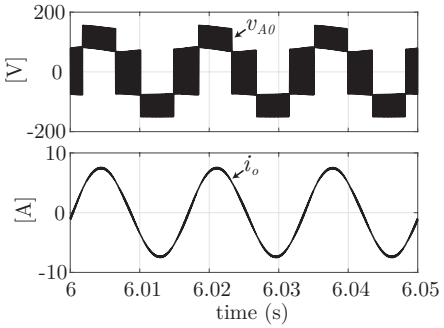


Fig. 7. Output voltage and load current.

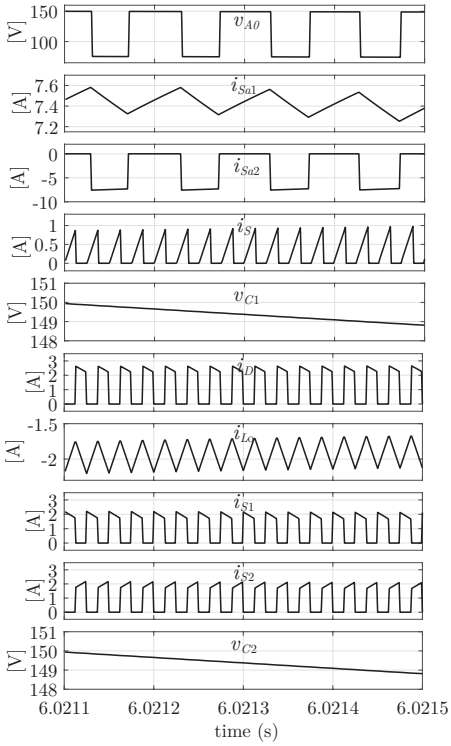


Fig. 8. Simulation results: different variables.

V. Experimental Results

In order to verify the feasibility of the proposed topology and its modulation strategy, a 450 VA single-phase five-level combined converter was tested using the setup shown in Fig. 11. Command signals of switches S_{a1} and S_{a2}, are shown in Fig. 12. It is shown from the top to the bottom of Fig. 13 that the combined converter is fed by a DC-link voltage of 300 V (top), obtained from an input voltage of 150 V, and a floating capacitor voltage of 75 V, as expected. Four levels have been obtained at the output voltage, thus resulting in the load current shown at the bottom of the figure. Note that the steps are not equally spaced. This is due to the relation between DC-bus and flying capacitor voltages. A relation of 1:3 equally spaces the steps.

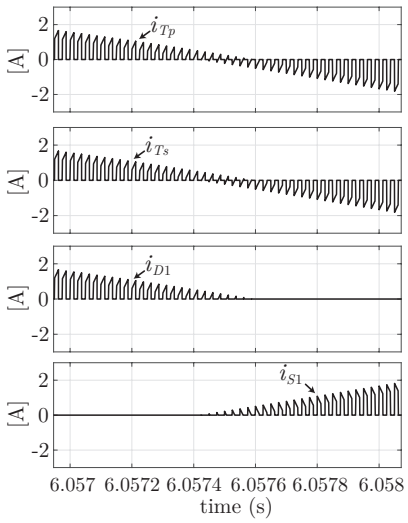


Fig. 9. Current i_{Tp}, i_{Ts}, i_{D1} and i_{s1}.

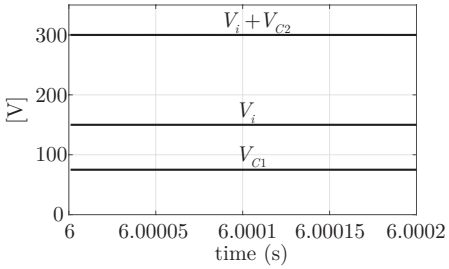


Fig. 10. DC-bus voltage, input voltage, and floating capacitor voltage.

VI. Comments

In the following the analyzed 4L-BFd-FC of Fig. 2 is compared with the 4L-CFC topology of Fig. 1(a) with the capacitor voltage regulated via PWM. It is considered that the 4L-CFC DC-bus is fed by the same rearranged boost converter used in the primary of the BF converter transformer. Table V establishes a comparison in terms of the number of switches, number of capacitors, number of magnetic and losses. It can be seen from Fig. 14 that losses are large in 4L-CFC with PWM regulation of the capacitor voltage (32.1 W) than in 4L-BFd-FC (27.2 W), which has the same number

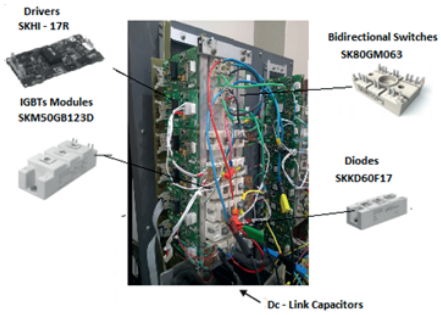


Fig. 11. Experimental setup.

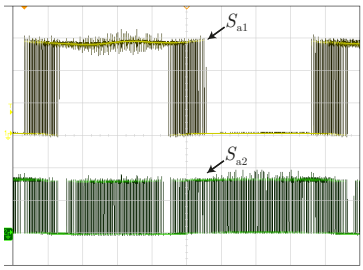


Fig. 12. Command signals for switches S_{a1} (top) and S_{a2} (bottom). 20 V/div.

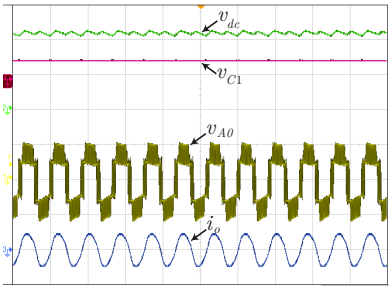


Fig. 13. From the top to the bottom: DC-bus voltage (100 V/div); floating capacitor voltage (100 V/div); output voltage (100 V/div); load current (20 A/div).

of switches but uses an additional transformer, thus increasing cost. In this investigation the use of either 4L-CFC or 4L-BFd-FC topologies seems to become a question of choice between cost and losses. However, cost calculation needs to be a accomplished for real conclusion. Also, other figures of merit should be examined for a final choice.

TABLE V
COMPARISON BETWEEN 4L TOPOLOGIES.

	4L-BFd-FC	**4L-CFC**
Switches	7	7
Capacitors	2	3
Reactor	2	1
HF Transformer	1	0
Total Losses/27.2 W	1 pu	1.18 pu

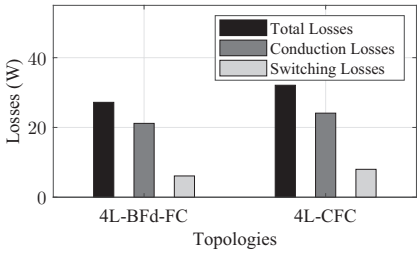


Fig. 14. Losses comparison.

VII. CONCLUSIONS

This paper investigated the use of a DC-DC high gain hybrid boost/forward converter to feed a single-phase FC inverter. The boost/forward converter employs only one winding and a single switch. Two of three its outputs were used, one to feed the DC-bus voltage and the other isolated one to regulate the flying capacitor voltage with a value different from half of the DC-link voltage, thus producing a four level voltage output. Simulation results are presented and verified by experimental results. Although the 4L-BFd-FC losses have been shown to be smaller than in case of the conventional 4L-FC inverter, its cost should be reduced so that become competitive.

ACKNOWLEDGMENT

Authors acknowledge the Conselho Nacional de Desenvolvimento Científico e Tecnológico (CNPq), from Brazil, for funding this investigation.

REFERENCES

[1] R. H. Baker and L. H. Bannister, "Electric Power Converter," Feb. 18 1975, United States Patent 3,867,643.

[2] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non conventional power converter for plasma stabilization," *Proc. of PESC'88*, pp. 212–219, 1988.

[3] G. S. Zinoviev and N. N. Lopatkin, "Evolution of multilevel voltage source inverters," in *9th International Conference on Actual Problems of Electronic Instrument Engineering*, vol. 1, 2008, pp. 125–136.

[4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, no. 5, pp. 518–523, 1981.

[5] H. Sugimoto, "New PWM control method for a three-level inverter," 1982, 80260 (Japan).

[6] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC'92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 397–403.

[7] X. Kou, K. A. Corzine, and Y. L. Familiant, "Full binary combination schema for floating voltage source multi-level inverters," in *IEEE Industry Applications Conference. 37th IAS Annual Meeting*, vol. 4, 2002, pp. 2398–2404.

[8] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 140–147, 2006.

[9] D.-Y. Lee, I. Choy, and D.-S. Hyun, "A new pwm DC/DC converter with isolated dual output using single power stage," in *IEEE Industry Applications Conference. 36th IAS Annual Meeting*, vol. 3, 2001, pp. 1889–1895.

[10] T.-J. Liang and K. Tseng, "Analysis of integrated boost-flyback step-up converter," *IEE Proceedings-Electric Power Applications*, vol. 152, no. 2, pp. 217–225, 2005.

[11] J. R. Dreher, F. Marangoni, J. L. Ortiz, M. L. d. S. Martins, H. T. Camara, and L. D. Flora, "High step-up voltage gain integrated DC/DC converters," in *IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2012, pp. 125–132.

[12] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Multi-output DC–DC converters based on diode-clamped converters configuration: topology and control strategy," *IET power electronics*, vol. 3, no. 2, pp. 197–208, 2010.

[13] J. C. Rosas-Caro, J. M. Ramírez, and P. M. García-Vite, "Novel DC–DC multilevel boost converter," in *IEEE Power Electronics Specialists Conference*, 2008, pp. 2146–2151.

[14] A. S. Andrade and E. R. da Silva, "DC-link control of a three-level NPC inverter fed by shaded photovoltaic system," in *13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, 2015, pp. 1–5.

[15] J. C. Giacomini, P. F. Costa, A. Andrade, L. Schuch, and M. L. Martins, "Desenvolvimento de um conversor CC–CC boost-forward integrado para aplicações com elevado ganho de tensão," *Eletrônica de Potência*, vol. 22, no. 2, pp. 206–214, 2017.

[16] F. Z. Peng, L. M. Tolbert, and F. Khan, "Power electronics' circuit topology-the basic switching cells," in *IEEE Workshop Power Electronics Education*, 2005, pp. 52–57.

[17] H. Wang, L. Kou, Y.-F. Liu, and P. C. Sen, "A new six-switch five-level active neutral point clamped inverter for pv applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6700–6715, 2016.